UNIT-2

PART-B

1. Explain how transistors act as a switch?
2. Explain the working of Depletion MOSFET.
3. Define fan-in and fan-out.
4. Draw the circuit diagram of NAND gate using CMOS logic.
5. Explain Diode logic.
6. Explain the operating principle of IIL gates.
7. What is Diode Logic? Explain with a truth table.
8. Draw FPGA Structure and explain the same
9. Write short notes on FPGA.
10. Why does the propagation delay occur in logic circuit?
11. State the advantage and disadvantage of CMOS family.
12. State the advantage and disadvantage of ECL family.
13. Define noise margin
14. What do you mean by logic level? Explain the positive logic and negative logic systems?
15. Mention the important characteristics of digital ICs

UNIT-3

PART-B

1. Write a HDL program for full adder using Dataflow modelling with a neat diagram
2. Explain the types of ROM Devices
3. Explain PoS with an example
4. What is PLA? Explain the working of PLA circuit.
5. Draw the truth table and explain the working of a half adder circuit.
6. Design HDL behavioural modelling of 4 to 1 line multiplexer.
7. Define combinational logic circuit. Give two examples.
8. Describe the working of a Decoder. Write its truth table.
9. Write a Gate level program for Full adder with a neat diagram
10. Difference between decoder and encoder
11. How does a priority encoder differ from an ordinary encoder
12. What do you mean by propagation delay?
13. What will be the maximum number of outputs for a decoder with a 6 bit data word?
14. What is a data selector
15. Describe the application of multiplexer

UNIT-2

PART-C

1. Describe the working of a TTL circuit

2. (i)Draw and explain two input NOR gate and NAND gate using NMOS LOGIC.

(ii) Design the following function using CMOS logic. F= AB + CD

3. With help of necessary diagrams explain the working of ECL logic.

4. Draw and explain following logic families: DTL (6) IIL (6)

5. Explain the operation of Enhancement and Depletion MOSFET with a neat Diagram

6. With help of necessary diagrams explain the working of TTL logic

UNIT-3

PART-C

1.(i)Explain the operation of 1:8 Demultiplexer with a neat diagram(6)

(ii)Implement the following function using 8:1 MUX (6)

F(A,B,C,D)=Σm(0,2,4,6,8,10,12,14)

2. Implement the following function using Quine Mc Clusky Procedure

F(A,B,C,D)= Σm(2,6,8,9,10,11,14,15)

3. Using a neat diagram describe the working of carry look ahead adder.

4. What is an Encoder and how does it work? Also note down the significance of priority encoder using necessary diagrams.

5.Explain Magnitude comparator with a neat diagram

6. Implement the following function using PLA.

F1= Σm (1,2,4,6) ; F2 = Σm (0,1,6,7) F3 = Σm (2,